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BURSTLOCK: A DIGITAL PHASE-LOCKED LOOP
USING BURST TECHNIQUES

by

COLAN MICHAEL ROBINSON

May 1977



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COLAN MICHAEL ROBINSON

May 1977

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1. INTRODUCTION

The past two decades have seen a revolution in the way in which information is processed. Today computers and computer technology are involved in almost every facet of our daily lives. The design simplicity, low cost and high reliability of digital circuitry developed for computer systems have produced an increasing trend towards the use of digital circuits in real-time applications, long the sole province of analog circuit techniques.

As a result, there has been a search for methods of digital data representation which can combine high speed and reliability with noise tolerance and low-cost processing elements. One proposed solution is that of unary processing, in which the value contributed by a bit of data is independent of its position. The data may be encoded either in a stochastic or deterministic manner. In unary processing, it is typical to employ averaging to improve the precision and noise immunity of the encoding.

This thesis will describe BURSTLOCK, a digital phase-locked loop implemented using a deterministic subclass of unary processing called Burst Processing. It is employed in a receiver to demodulate commercial FM broadcasting. It will be shown that BURSTLOCK provides a number of advantages over conventional phase-locked loops, both practically, as it consists of only a small number of digital components, and theoretically, by reducing the interdependence of loop parameters to provide a broader range of design tolerance when attempting to maximize conflicting quantities.

2. THE PHASE-LOCKED LOOP

2.1 Introduction and Background

A phase-locked loop (PLL) is a feedback system which attempts to synchronize a voltage-controlled oscillator (VCO) with an input signal. Figure 2.1 gives a basic block diagram of the PLL, which consists of a phase comparator (PC), low pass filter, amplifier and VCO.

With zero input, the VCO operates at a set frequency referred to as the "quiescent frequency" (f_Q). The phase comparator produces an output that is proportional to the phase difference between the input and VCO signals. This output is filtered, amplified and applied to the control input of the VCO, forcing the VCO frequency to vary in the direction that will decrease the phase difference between the two signals. If the difference between the input frequency and the quiescent frequency is sufficiently small, the VCO will be forced closer to the input frequency until the two frequencies are equal. When this occurs the loop is said to be "in lock." The range of frequencies over which this locking behavior can occur is called the "capture range."

If the input frequency changes once the loop is locked, the VCO will follow the change due to the feedback properties of the system, as long as the deviation of the input is not too large. The range of frequencies over which the PLL will remain locked is called the "lock range."

It is necessary that a phase difference between the input and VCO signals is maintained in order to generate a control voltage sufficient

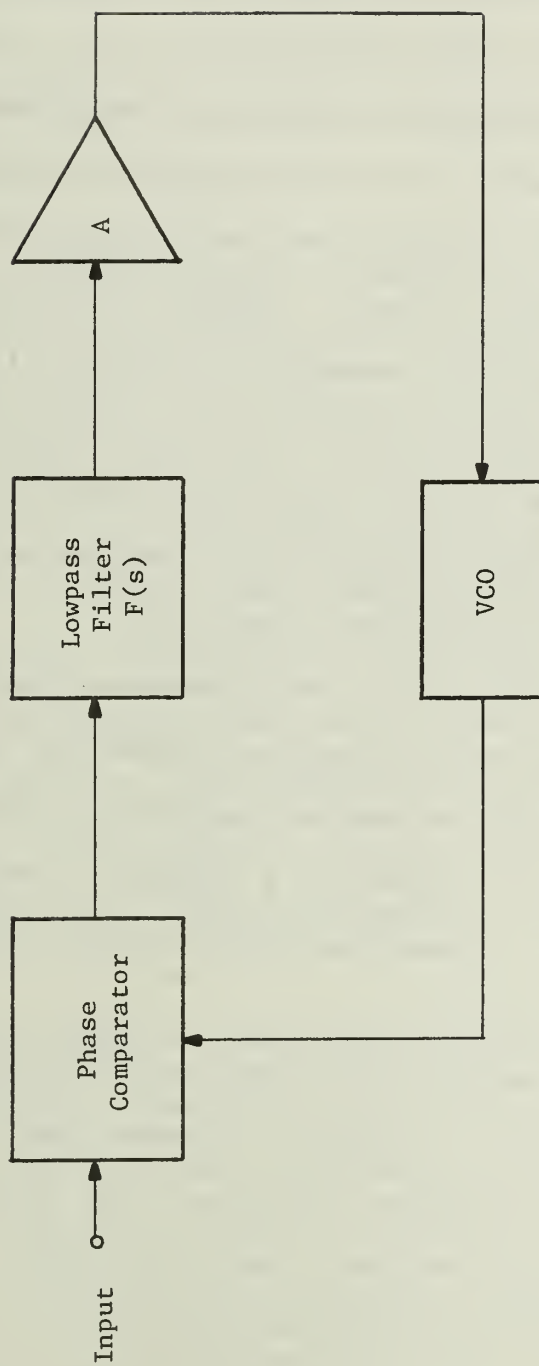


Figure 2.1 Basic Phase-Locked Loop

to shift the VCO from f_Q to the lock frequency. This static phase error is inversely proportional to the gain around the loop, represented in the diagram by an amplifier with gain A, where A represents the change in VCO frequency per unit phase error.

Descriptions of phase-locked loops can be found dating back to the twenties and thirties. However, the first important practical application came in the early fifties, when PLL's were used to reconstitute the color subcarrier in color television signals. "Flywheel" synchronization used the property that if the input is removed, the VCO will drift away only slowly from the lock frequency. Thus the color oscillator at the receiver can be synchronized to that at the transmitter by locking on to a short color burst transmitted once each frame, and relying on the memory of the loop to coast through the period between bursts [9].

The application of the PLL to radio reception became important with the inception of the American space program. Narrow band signals transmitted from a satellite could be received despite uncertainty about the signal frequency, which could range over a frequency interval 1000 times the signal bandwidth due to transmitter drift and Doppler shift, because of the tracking action of the PLL.

At the present time the PLL is widely used for demodulation in high quality FM receivers due to its superior performance over a conventional discriminator. In this application the output of the system is the filtered output of the phase comparator, which corresponds to the program signal as it forces the VCO to follow the modulation of the carrier.

By inserting a frequency divider in the feedback loop between the VCO and the phase comparator, the PLL functions as a frequency multiplier.

It can also act as a frequency translator by adding an offset voltage to the VCO control input.

The PLL can be made to lock on to only one of several signals at its input by setting f_Q of the VCO correspondingly. The undesired frequencies are attenuated, thus improving the signal-to-noise ratio.

2.2 PLL Components

The phase comparator closes the feedback loop, producing an output which depends on the phase difference between the input and the VCO signal. Since it cannot distinguish between different cycles of the signals, its output must be a periodic function of the phase difference, with period equal to 2π radians. Most practical phase comparators have an output that is directly proportional to the sine of the phase error. However, the sinusoidal nonlinearity of the phase error ϕ_E is usually disregarded by assuming a small ϕ_E so that the loop operates in the region where $\sin \phi_E$ is approximately equal to ϕ_E . This assumption is accurate to within 5% for $\phi_E < \pi/6$. Since the PC converts a frequency difference into a phase difference, and phase is the integral of frequency, the PC functions as an integrator.

It is necessary that the VCO be highly linear over a wide range, with high phase stability. Depending on the application certain requirements may be sacrificed to improve others, as there is conflict between them.

The order of the loop is equal to the number of finite poles in the open-loop transfer function. A first-order loop contains no filter. (The integrating action of the PC contributes one pole.) Second-order loops, which contain one integrator, are the most common. High-order loops are very sensitive to circuit parameter changes, difficult to stabilize and

unnecessary in most PLL applications. The lowpass characteristic of the filter $F(s)$ attenuates fast changes in the phase error due to noise or phase jitter in the input signal.

The amplifier shown in Figure 2.1 may or may not be physically present and simply represents the combined dc gain of all the components in the loop.

2.3 PLL Parameters

The lock range R_L is the distance from f_Q that the VCO, once locked, can be moved while still maintaining lock. For a linear phase comparator, the lock range is equal to πA radians per second [5]. For a sinusoidal phase comparator, since the sine function cannot exceed 1, the lock range is equal to A radians per second [2]. This value will be used for further derivation, following the convention in the literature [2,5,12]. The capture range R_C is the maximum distance from f_Q that the loop will lock on to an input signal from an unlocked state. R_C is always less than or equal to R_L .

It should be pointed out that when a frequency step is applied to the input of a locked loop, the loop may lose lock for a few cycles if the frequency variation is too large, even though it remains within R_L . There is a maximum rate of input frequency change for which the loop will not lose lock temporarily. For a second-order loop, by applying the final value theorem to the expression for the phase error, this rate may be shown to be equal to the square of the natural frequency of the filter (units of radians per second per second) [2].

As mentioned above, when the loop is locked, there is a static phase error required to keep the VCO at the lock frequency. In many cases

a small phase error is desired, but for discriminators, where this phase error is the output, this is not necessarily the case. For a first-order loop with a lock frequency f_L and a quiescent VCO frequency f_Q , the static phase error is $(f_L - f_Q)/A$. The phase error can be reduced to zero by using a third-order loop [12].

Another useful loop parameter is the loop bandwidth B_L , which is defined as the 0 dB frequency of the open-loop gain. For a first-order loop or a second-order loop with cutoff frequency greater than B_L , the gain decreases with frequency at 6 dB/octave due to the $1/s$ term provided by the integrating action of the PC, and thus $B_L = A$. In this case $R_L = R_C$. For FM detection, B_L must be large enough to track the modulation. However, the bandwidth should be as small as possible to attenuate noise in the input. Any change in B_L will also affect R_L and R_C , since all these quantities depend on A .

If the cutoff frequency of the low-pass filter is reduced below A , the attenuation of noise can be increased while keeping R_L the same. However, there is a penalty to be paid for the decrease in B_L . The system response to an input frequency change becomes an underdamped ringing. Also R_C is reduced. For a simple RC filter the reduction in R_C is approximately equal to the reduction in B_L caused by the decrease in filter bandwidth. Using a lag network filter the reduction in R_C is approximately equal to the square root of the B_L reduction [5]. Moschytz [7] has derived a general parametric approximation to R_C : $R_C = A|F(R_C)|$. Since $F(R_C)$ cannot be greater than unity, R_C cannot be greater than R_L ($R_L = A$). Note that the gain of an active filter is included in A .

It is often convenient to think of a PLL as acting as a bandpass filter on the input signal, as in the satellite communications application described above. The filter has a center frequency equal to the input frequency and a noise bandwidth B_N on each side. For a first-order loop $B_N = A/4$ Hz. For a second-order loop with $F(s) = 1 + a/s$, $B_N = (A+a)/4$ [12].

In most applications it is desirable to have both a wide R_C and a narrow B_N . It can be seen, however, that these requirements conflict with each other.

2.4 Capture Behavior

The capture behavior of a PLL is extremely complicated and difficult to describe mathematically. However, it may be easily understood in a qualitative manner.

Consider a first-order loop with a linear phase detector. For the first-order loop $R_L = R_C$. Figure 2.2 describes the operation of the loop [5]. The VCO frequency appears on the vertical axis and the phase difference between the VCO and the input signal on the horizontal axis. Each curve represents the VCO frequency as a function of the phase difference for a particular choice of f_Q , and is periodic in 2π . The horizontal axis represents the frequency of the input signal. Thus locking can occur only if the curve for a given f_Q intersects the axis. For example, the curve for f_{Q3} crosses the axis twice in the interval 0 to 2π . As shown, only one of these intersections is stable, the other corresponding to positive rather than negative feedback. The distance from the vertical axis to the intersection is the static phase error. The lock range can be seen to be $(f_{Q4} - f_{Q2})/2$. If the VCO operates at f_{Q1} , lock cannot be achieved. The operating point will move along the curve in the direction of the arrow, producing frequency modulation.

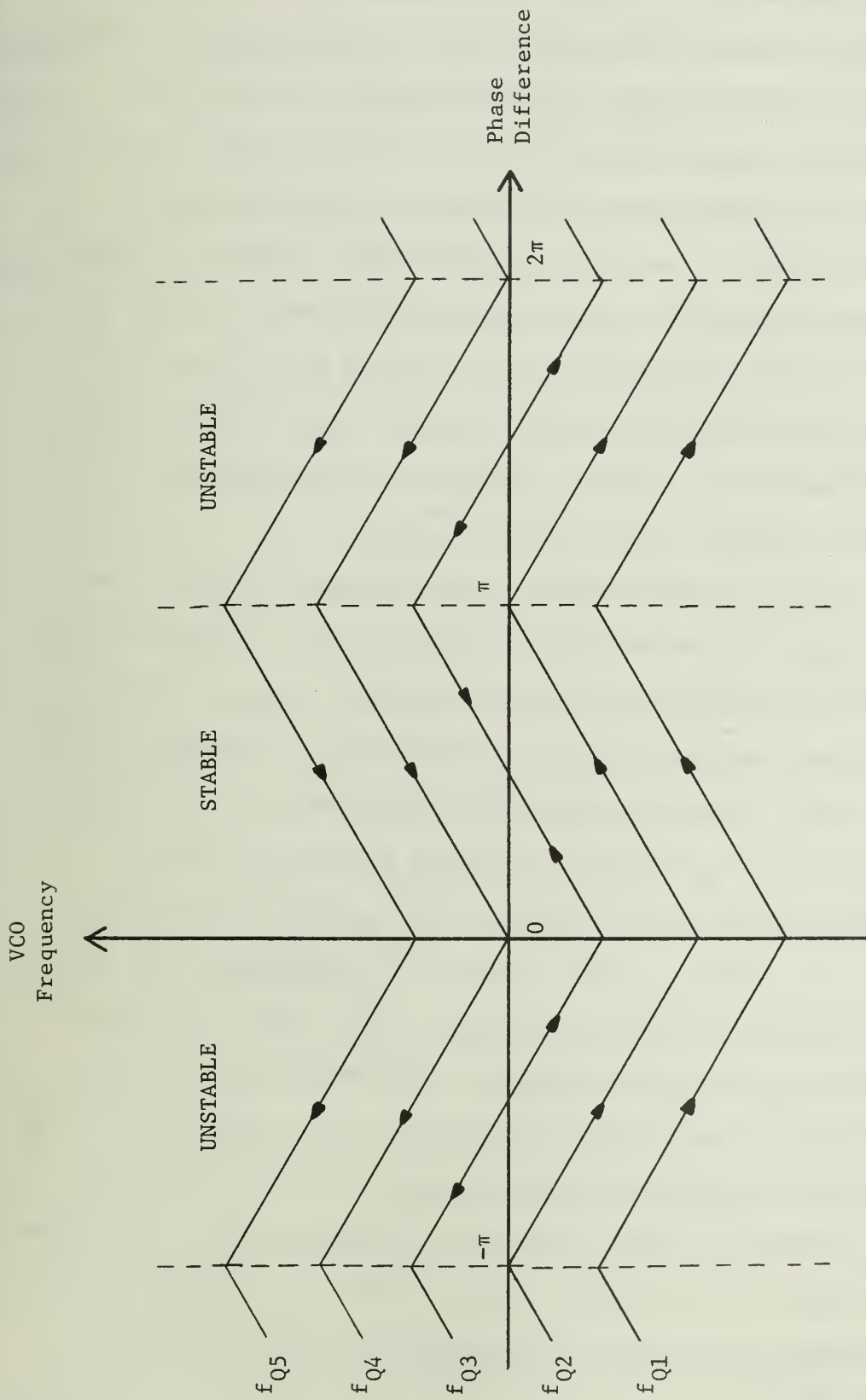


Figure 2.2 PLL Operation

It is instructive to consider the operation of the loop when the input frequency is outside the capture range, as on the f_{Q1} curve. Since the VCO and input frequencies are different, the output of the phase comparator is a beat frequency. If the VCO is modulated away from the input frequency the beat frequency increases and the operating point moves rapidly, whereas if the VCO is modulated toward the input frequency the beat frequency decreases and the operating point moves more slowly. The output of the phase comparator can be shown [5] to be a series of back-to-back exponential curves with flat regions as the operating point hesitates at its closest approach to the input frequency, and sharp cusps as the VCO moves rapidly at its furthest excursion.

When the more common sinusoidal phase comparator is used, the triangular shape of the curves becomes sinusoidal, but the operation will be similar otherwise [2,12]. So far, the first-order loop, in which $R_L = R_C = B_L$, has been described. The discussion may be extended to the second-order loop. If the frequency difference between the VCO and input signals is less than B_L , locking will proceed directly and almost instantaneously, as in the first-order loop [2]. When the operating point does not intersect the input frequency axis the phase error looks like a series of cusps as before. Because of the asymmetrical shape of the waveform, it contains a dc component. This was why the first-order loop tended to linger at its closest approach to lock. The filter in the second-order loop integrates this dc component, pushing the VCO closer to the input frequency. For a second-order loop with a perfect integrator the capture range is theoretically infinite. With a more normal type of loop filter the capture range is proportional to the filter response as already described.

Viterbi [12] has used an analog computer to produce a number of curve families of the type in Figure 2.2 for second-order loops with different filter characteristics. These curves show a spiral tendency in the path the operating point takes due to the underdamped ringing described above.

A study of the capture behavior of a PLL leads to another quantity used to characterize the loop: the "capture time" T_C . This is the time taken for the loop to lock once the input signal is applied. For a first-order loop, if capture is possible, T_C will be on the order of $1/A$ seconds [2]. For a second-order loop with a loop filter characterized by a natural frequency ω_N and a damping factor ζ , if the input signal is within B_L then T_C is of the order of $1/\omega_N$ seconds. If this condition is not true, an explicit formula for the capture time is somewhat difficult to derive. Gardner [2] gives an approximation derived by Viterbi for a difference between input frequency and VCO frequency of $\Delta\omega$ radians/second: $T_C = \Delta\omega^2 / (2\zeta\omega_N^3)$. Thus acquisition is faster with a wider loop bandwidth. Note that if the VCO had previously been tracking another frequency, $\Delta\omega$ would be measured from the VCO frequency, not from f_Q . Thus R_C extends on either side of the current VCO frequency, but cannot exceed the limits of R_L which is centered on f_Q .

The capture time can be exceedingly long if $\Delta\omega$ is large compared with A or B_N . As an example [2], consider a high-gain second-order loop with $\zeta = 0.707$, a commonly selected value, and a frequency difference of Δf Hz. Gardner shows that T_C is approximately equal to $4.2 (\Delta f)^2 / B_N^3$ seconds. For a narrow-band loop with $\Delta f = 1$ KHz and $B_N = 10$ Hz, $T_C = 1$ hr. 10 min.!

Because of such long capture times a commonly used technique in this type of situation is to apply a sweep voltage to the VCO to search

for the input frequency. The maximum sweep rate is limited by B_N [12]. Once lock has occurred the sweep voltage must be removed. Otherwise, if the input signal fades out momentarily, the VCO will be carried away from the lock frequency. Locking during sweep is by no means certain and the loop must be designed carefully to give a high probability of capture [2].

2.5 Further Considerations

If the input signal to a first-order loop fades out, the VCO will return to f_Q . In a second-order loop, because of the integration of the filter, the VCO frequency will tend to remain the same. Thus the loop may be said to have memory. With a perfect integrator, the frequency will never change. Using a realistic filter, the holding time is proportional to the gain of the filter. This property is used in flywheel synchronization as described above.

Some mention should be made of the relatively uncommon third-order loop. Analysis is much more complex than the second-order case. Design is also more complicated as the third-order loop is only conditionally stable, whereas first and second-order loops are unconditionally stable. However, the third-order loop is advantageous in some applications. The addition of a second integrator also gives the loop an acceleration memory. If the input signal has a constant acceleration, such as a Doppler shift, when the signal fades out the loop will continue to track at the same rate of change of frequency. This is particularly useful in space communications.

A PLL is by no means the best way to measure the frequency of a constant input. Its principal advantages are its ability to track the frequency of a varying input and to improve the signal-to-noise ratio.

3. BURST REPRESENTATION

Burst representation is a method of encoding information in pulse form proposed by Professor W. J. Poppelbaum as a middle ground between weighted binary and stochastic representations [10]. It retains the noise tolerance and processing simplicity of stochastic schemes while offering increased precision and speeds approaching that of weighted binary.

In essence, Burst representation is a unary (unweighted) encoding. A serial pulse stream is viewed as a sequence of n -bit blocks. The value of each block is defined to be the fraction of the number of 1's in the block to the total number of slots, and can vary between 0 and 1. If negative numbers are required, they may be mapped into the range of the representation, as in two's complement binary encoding, or a sign bit may be transmitted separately. As the blocks pass through an n -bit shift register, the value represented in the register provides an interpolation between the values of successive blocks and thus is valid at all times. No synchronization is necessary.

By selecting a value of n , the designer may trade off precision and speed. The philosophy behind Burst processing is to select a low n (typically 8 or 10) so that processing elements are simple and inexpensive, and to obtain increased accuracy by averaging the result. The practicability of this technique in a number of applications has been demonstrated by members of the Information Engineering Laboratory.

Decoding of Burst encoded information is accomplished by a block sum register (BSR), which is an n -bit shift register, each stage of which controls a unit current source. The currents are summed on the output bus to provide a quantized analog output proportional to the Burst value contained in the register. Figure 3.1 shows a 5-bit BSR which contains the value 0.6. Bursts may also be converted into weighted binary by the use of a simple up-down counter.

As the BSR acts as an integrator with a finite memory, it is not surprising that higher frequencies are attenuated by a low pass filtering action. Obviously, with a clock frequency of f_C , frequencies higher than $f_C/2$ cannot be represented at all. Since the value in the BSR is constrained to change by only $1/n$ in each clock period, a limit is placed on the maximum amplitude at a given frequency. The cutoff frequency of a BSR has been defined by Taylor [12] to be $f_C/2n$. At the cutoff frequency the maximum amplitude of a signal is $2/\pi$.

There is no requirement that the 1's in a block be contiguous, although this may be advantageous in certain applications. If this is so, it is termed a "compacted" Burst. A particular class of uncompacted Bursts which will be of interest is Delta Block Encoding (DBE), which is analogous to conventional delta modulation. In this case the serial inputs of a bidirectional BSR are tied to logical one and logical zero, and the Burst input controls the direction in which the BSR shifts. In each clock period the value in the BSR is either increased or decreased by $1/n$ to correspond to the changing value of the encoded signal.

One obvious disadvantage of this scheme is that there is no way to encode a constant value--the closest approximation gives granular noise with an amplitude of $1/n$. This can be remedied by providing two

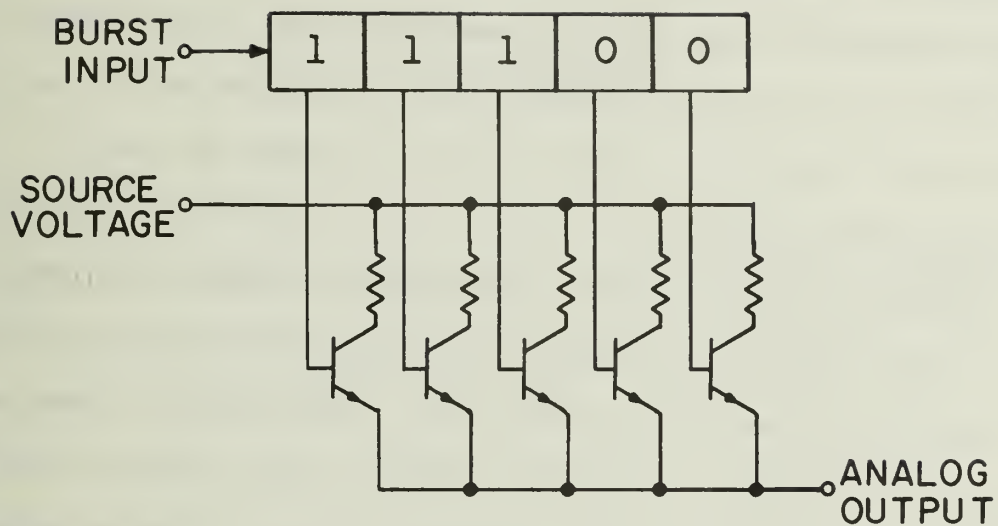


Figure 3.1 A 5-bit BSR

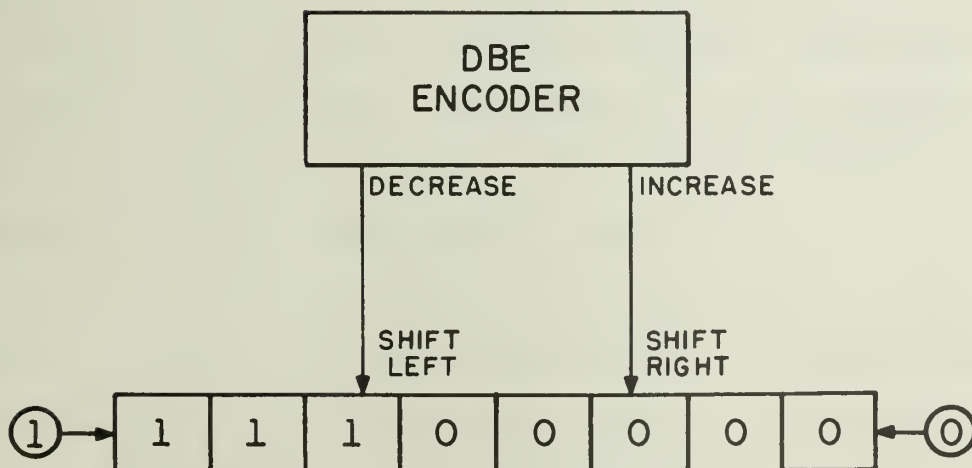


Figure 3.2 Decoding a Tristate DBE-Encoded Burst

control lines, one to increase the value in the BSR and one to decrease it. If both lines are inactive, the BSR value remains constant. (The situation in which the lines are simultaneously active is not permitted.) This encoding will be termed "tristate" DBE, as there are three possible actions to take in each clock period. Figure 3.2 shows the means by which tristate DBE is decoded.

Although in some situations it may not be considered worthwhile to use two lines instead of one merely to remove a small amount of noise (which could just as easily be filtered out), this encoding is vital to the concept of BURSTLOCK. In this case, the two control signals do not originate at a single encoder which encodes an externally derived signal, but rather are produced separately in order to encode the relationship between two external signals.

4. THE BURSTLOCK CIRCUIT

4.1 BURSTLOCK Operation

BURSTLOCK is a phase-locked loop designed using burst techniques [8]. From the discussion above, it should be clear that the design of a PLL depends largely on the intended application. The BURSTLOCK circuit constructed was designed for FM demodulation, and in conjunction with appropriate reception and output circuits forms a receiver that will pick up commercial FM broadcasting. It will be shown that the BURSTLOCK design has certain theoretical advantages over conventional PLL's.

Figure 4.1 shows the BURSTLOCK circuit. The system clock is not shown on the diagram, but should be understood to input to all counters and shift registers. All clocked components are positive edge-triggered.

Since all the information in an FM signal is contained in the frequency, the waveshape may be adjusted to any convenient form. The input signal is represented here by a pulse one clock period long produced when the sinusoidal broadcast signal passes through zero with a negative slope. The zero-crossing detector synchronizes the pulse with the system clock. This signal is denoted EXT ZERO (external zero).

The VCO in the conventional PLL corresponds here to a local oscillator consisting of a local oscillator counter, a comparator and an averaging counter. The averaging counter controls the period of the oscillator, and is adjusted to follow the variation of the input signal. It may be considered to contain the average value of previous input periods over some finite time interval. The local oscillator counter is set to

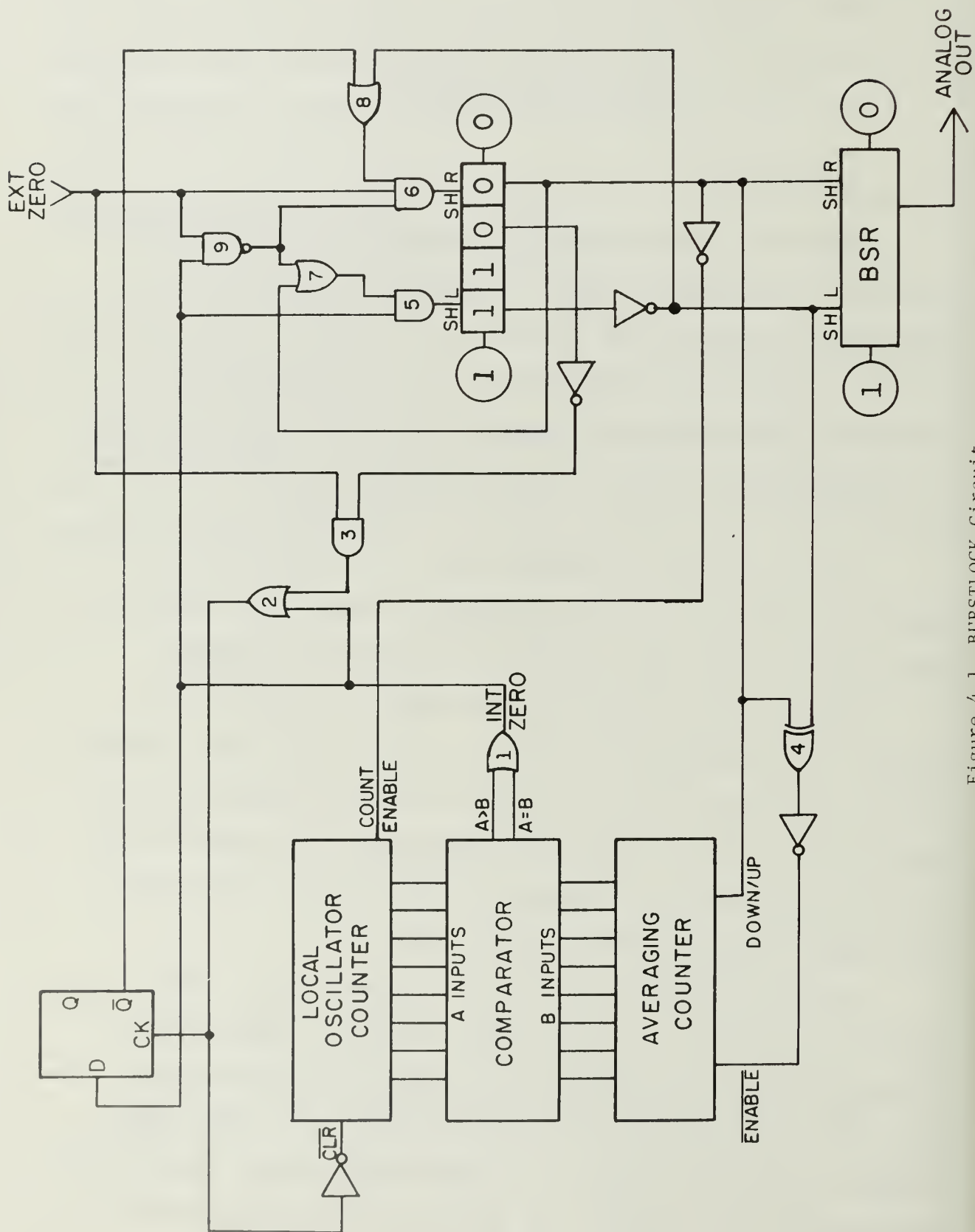


Figure 4.1 BURSTLOCK Circuit

zero at the beginning of a period and counts up until it is equal to or greater than the value in the averaging counter, whereupon it is reset to zero. Note that it is not sufficient to reset the local oscillator counter solely when it is equal to the averaging counter, because if the averaging counter is decremented during the same clock period that the local oscillator counter is being incremented to equal the old value, equality will never occur. The output of gate 1 is considered the output of the local oscillator, and is termed INT ZERO (internal zero). It has the same format as EXT ZERO, that is, one pulse per oscillator period. Since the local oscillator count begins at zero, the value in the averaging counter will be one less than the period of the local oscillator (measured in clock periods).

The operations of phase comparison and lowpass filtering are combined in the balance register, a bidirectional shift register with length n_B bits denoted $B(0) \dots B(n_B-1)$. The left serial input is tied to logical one, and the right to logical zero. The balance register is thus a decoding register for a tristate DBE-encoded burst. As a first approximation to its action, the shift left control input is INT ZERO and the shift right EXT ZERO. The local oscillator is cleared whenever either INT ZERO or EXT ZERO is high. Thus, in contrast to the conventional PLL, the phase comparator can distinguish between different cycles of the signals and the response is not periodic in 2π .

Consider the case when the local oscillator has just been cleared by EXT ZERO. Then if EXT ZERO is the next signal to go high, the value in the balance register is increased by one, indicating a positive phase error, that is, the frequency of the local oscillator is too low. If EXT ZERO

and INT ZERO go high simultaneously, gate 9 disables both the shift left and shift right control inputs. (If both were high simultaneously the register would load from the parallel inputs.) The value in the balance register remains constant, and the loop is in lock.

If INT ZERO goes high first, the value in the balance register is decreased by one, indicating a negative phase error, that is, the frequency of the local oscillator is too high. Without further modifications, the next pulse on EXT ZERO would simply return the balance register to its previous value. To solve this problem, a D flip-flop is included in the design. Its value is updated every time the local oscillator is cleared, either by INT ZERO or EXT ZERO, and it is set to the value of INT ZERO. Thus in the case being discussed, the pulse on INT ZERO sets the flip-flop. The \bar{Q} output then goes low, thereby blocking the next pulse on EXT ZERO through gate 6 and preserving the decrementation of the balance register. The circuit is now returned to the initial conditions of the discussion. Note that if the phase error is less than $-\pi$ (the local oscillator is more than twice the input frequency), the balance register will be decremented more than once. This demonstrates the claim that the phase comparison is not periodic in 2π .

The value in the balance register is updated by only one bit per cycle of the higher frequency signal. Thus the comparator output has a precision of only one bit for every π radians of phase error. (Here "bit" is used in the burst sense of the number of positions that can be filled, not in the meaning used in information theory.) To obtain improved performance, the burst philosophy of averaging over a longer time period is employed, using the integrating action of the balance register. $B(0)$

and $B(n_B-1)$ are monitored, and only when the balance register is at its maximum or minimum value is the averaging counter (and thus the frequency of the local oscillator) altered. Since EXT ZERO is synchronous with the clock, whereas the external signal from which it is derived is extremely unlikely to be harmonically related to the clock frequency, there will always be some phase jitter in EXT ZERO. This jitter is removed by the loop.

If there is a consistent negative phase error, the integrated value in the balance register will eventually be reduced to zero the clock period after a pulse on INT ZERO. The $\overline{\text{COUNT}}$ input of the averaging counter goes low, enabling counting. $B(n_B-1)$ is low so the counter will count upwards. Since the local oscillator was just cleared, and the two counters count up at the same rate, the local oscillator can never clear. The averaging counter will continue to be incremented every clock period until the clock period after that in which EXT ZERO goes high. Although the flip-flop operates as before, $\overline{B}(0)$ overrides the operation of this part of the circuit by passing a logical 1 through gate 8, enabling the EXT ZERO signal through gate 6 to shift the balance register right one bit, halting the upward count of the averaging counter. At this point the local oscillator frequency will be exactly equal to the frequency of the input signal, and the loop will be in lock.

If there is a consistent positive phase error, the integrated value in the balance register will eventually reach n_B on the clock period after a pulse on EXT ZERO. $B(n_B-1)$ will go high, disabling the incrementation of the local oscillator counter. Since $B(n_B-2)$ was set high by the previous EXT ZERO pulse, the local oscillator counter was not reset by the later pulse due to the action of gate 3, and stands at one more than the correct

value. During each succeeding clock period the value in the averaging counter is decreased by one until it becomes equal to the value in the local oscillator counter, at which point INT ZERO goes high. At the next clock period, the local oscillator counter is reset, the value in the balance register is decreased by one, and the value in the averaging counter is decreased by one to the correct value, leaving the loop in lock. The next pulse on EXT ZERO will synchronize the local oscillator to the input signal. The balance register will not change because the pulse on INT ZERO set the flip-flop. A phase error greater than π radians can be corrected because a pulse on EXT ZERO while the correction is taking place will not reset the local oscillator counter, and cannot change the balance register because it is already at its maximum value. If the pulse on INT ZERO is coincident with a pulse on EXT ZERO, the balance register will still be decremented as $B(n_B-1)$ is high, enabling the INT ZERO signal to the shift left control input of the balance register through gates 7 and 5.

The output of the circuit when it is used as an FM demodulator is provided by a second bidirectional shift register acting as a decoder for a tristate DBE-encoded burst. The inputs are $\bar{B}(0)$ and $B(n_B-1)$, the correction pulses for the averaging counter. By integrating these signals, the filtered phase detector output, and thus the modulation of the input frequency, can be obtained. By making this register a BSR the output is available in an analog form suitable for audio output.

4.2 BURSTLOCK Parameters

The first difficulty in describing the operation of BURSTLOCK is defining what it means for the loop to be in lock, particularly when the

input frequency is changing. For any digital PLL, operating in discrete time, any change in the input frequency cannot be compensated immediately, so that the loop may strictly be said to have lost lock. The situation is similar to that of the conventional PLL when the input frequency changes at higher than the maximum allowable rate and the loop unlocks for a few cycles until it can catch up with the input again. Even for the conventional PLL there is some theoretical difficulty in defining lock in other than a statistical sense [2]. However, for discussion purposes it is sufficient to say that the BURSTLOCK circuit is "strictly locked" when the local oscillator frequency is exactly equal to that of the input, and unlocked when it is unable to move the local oscillator into strict lock.

Let the local oscillator counter and the averaging counter have length n_L bits, and the system clock frequency be f_C Hz. Then the lock range is unconditionally equal to the capture range, and is the range of frequencies from $f_C/(2^{n_L}-1)$ to $f_C/2$ Hz. Note that since the local oscillator has no quiescent frequency, the lock range cannot be defined as a deviation from the quiescent frequency as in the conventional PLL, but is instead an absolute quantity.

The absence of a quiescent frequency means that when the loop is strictly locked there is no need for a constant signal to displace the local oscillator. Thus the static phase error is always zero.

The concepts of loop gain and bandwidth are somewhat troublesome to define. This difficulty is due to the fact that BURSTLOCK is not an attempt to transform a conventional PLL component by component into digital form. Therefore, a one-to-one correspondence of system characteristics is not to be expected.

Taylor [11] has defined the cutoff frequency of an n -bit BSR as $f_C/2n$, the point at which the maximum amplitude of the input signal has fallen by a factor of $2/\pi$. Since the value of a burst-encoded signal is constrained to change by only one bit every clock period, higher frequencies must necessarily be attenuated by the nature of the encoding. However, this result is not directly useful in describing the filtering operation of the balance register, since only the rightmost and leftmost bits are examined.

Instead, consider the operation of the balance register. The value can only be changed once for each period of the higher frequency of INT ZERO and EXT ZERO. For the signal to appear at all the value of the balance register must vary from 0 to n_B and back, requiring $2n_B-1$ alterations. For this to occur, however, the input frequency must be changing, so the alteration of the balance register does not take place at a constant rate. Suppose that the input signal is being modulated by a square wave between the frequencies f_1 and f_2 , $f_1 < f_2 < f_C/2$. Then the frequency of the modulation that can possibly appear at the output lies between $f_1/(2n_B)$ and $f_2/(2n_B)$. Choosing the safer alternative, the bandwidth of the balance register may be defined as $f_1/(2n_B)$. Note the similarity in form to Taylor's result.

The capture time is defined to be the time taken for the local oscillator to move from strict lock at f_1 to strict lock at f_2 when the input signal undergoes a step frequency change from f_1 to f_2 . From the operation of the circuit it can be seen that the path taken is always direct--there is no underdamped oscillation. The capture time depends to some extent on the past history of the circuit. If no noise is present

in the input, when the loop is in strict lock the value contained in the balance register will be either 1 or $n_B - 1$, depending on the direction from which lock took place. Thus, denoting the period corresponding to f_1 as p_1 , and f_2 as p_2 , the capture time will be either $|p_1 - p_2|/f_C + \min(p_1, p_2)/f_C$ or $|p_1 - p_2|/f_C + (n_B - 1) \min(p_1, p_2)/f_C$. In the limit, therefore, T_C is inversely proportional to the system clock frequency and directly proportional to the period difference. When the linearizing assumption to be discussed in detail below is employed, the capture time may be said to be linearly proportional to the frequency difference.

The previous discussion of the balance register value in strict lock may be described by saying that the circuit expects the input frequency to continue changing in the same direction that the loop has previously been tracking it. If the input frequency moves in the opposite direction the local oscillator will not follow for $n_B - 1$ cycles of the higher frequency. Therefore, the recovered signal modulation will have flattened peaks due to this integrating action of the balance register. The distortion increases as the filter bandwidth is reduced, i.e., as n_B is increased, and of course is more severe with higher-frequency modulation. This is not an unexpected result, since if high frequency noise is attenuated by the filtering action the higher-order harmonics of the modulation corresponding to rapid changes in the input frequency will also be attenuated. For sinusoidal modulation at a frequency f_M of the input, with the lowest excursion of the input frequency at f_1 , distortion is less than 5% if $2n_B f_M < .05f_1$. In general, distortion of $d\%$ or less will be obtained if $2n_B f_M < df_1$. This approximation is valid for $d < 30\%$.

BURSTLOCK differs from the conventional PLL in its behavior when the input signal drops out. The balance register gives the circuit some memory, and it will stay at the lock frequency for between 1 and $n_B - 1$ cycles, as already discussed. As the memory of a conventional PLL evaporates, the VCO returns to f_Q . The BURSTLOCK local oscillator, having no f_Q , interprets the signal dropout as the input frequency being modulated to zero and attempts to track. Since n_L is finite, the averaging counter will eventually overflow, setting the local oscillator back to its maximum frequency and forcing the search to continue. Because of this behavior, and the small lower bound on frequency memory, BURSTLOCK is not suitable for flywheel synchronization applications, although input signal dropout for only a few cycles can be tolerated. However, for FM demodulation, the continual increase in the averaging counter will quickly saturate the output BSR, giving a dc output. Thus for this application the output is similar to a conventional PLL returning to its quiescent frequency.

4.3 The BURSTLOCK Receiver

Figure 4.2 shows the means by which commercial FM broadcasts are encoded into a form suitable for demodulation by BURSTLOCK. The output of the encoder is used as the EXT ZERO input for a BURSTLOCK circuit with $n_B = 4$ and $n_L = 8$. The tuning of a station is done by an inexpensive commercially built FM tuner. (David Wells of the Information Engineering Laboratory is currently investigating digital tuning methods.) The 10.7 MHz IF output of the tuner is mixed down to 200 KHz to enable the use of moderate speed digital circuitry for the demodulation. (Standard TTL was used.)

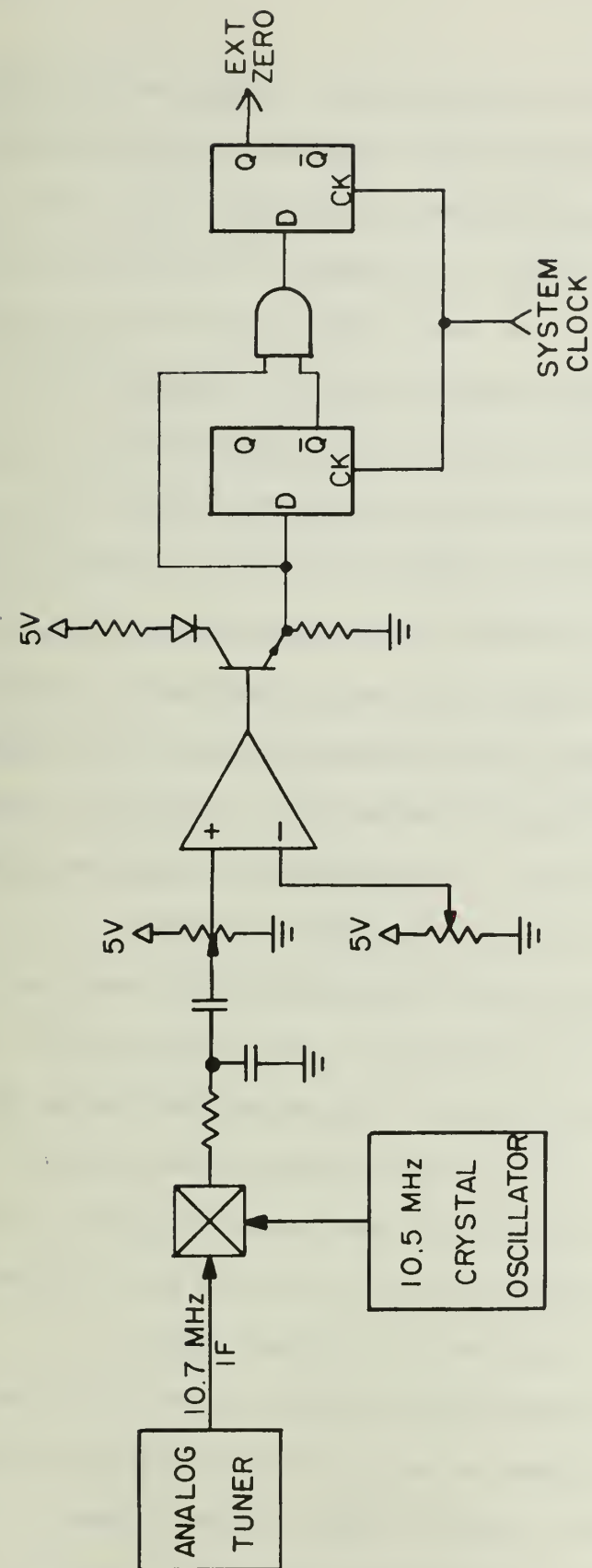


Figure 4.2 BURSTLOCK Input Encoding

The FM signal is applied to one input of a comparator, the other input of which is a dc level adjusted to the middle of the FM sinusoid. The comparator output drives the input of a D flip-flop. The \bar{Q} output of the flip-flop is ANDed with the input. The output of the flip-flop will be a pulse that occurs only when the input changes from zero to one, that is, when the input signal passes through zero with a negative slope. A second D flip-flop synchronizes the pulse with the system clock.

An analog audio output is provided by the output BSR of the BURSTLOCK circuit. If the BSR has a length of n_0 bits, its signal-to-noise ratio (SNR) will be $2n_0$. This assumes that the signal varies from zero to the maximum value. If the signal has a smaller amplitude, since the quantization noise is constant, the SNR will deteriorate. If the signal amplitude is larger than the register length, clipping will occur. Thus it is of interest to discover how to obtain the optimum amplitude of the BURSTLOCK output. This may be simply calculated as follows.

Suppose that the input signal is being modulated between the frequencies f_1 and f_2 , $f_1 < f_2$, with periods p_1 and p_2 respectively. Then with an output BSR of length n_0 bits, the optimum amplitude may be obtained by setting $f_c = n_0 / (p_1 - p_2)$ Hz. Since the frequency of the receiver IF output is difficult to set exactly at 10.7 MHz without monitoring it with a frequency counter, the BURSTLOCK receiver is provided with a variable-frequency clock so that fine adjustments may be made aurally.

The BURSTLOCK circuit demodulates a frequency-modulated input by integrating the corrections needed to keep the local oscillator tracking the input frequency. A single correction pulse produces a change in local oscillator period equal to one clock cycle, rather than a standard step

frequency change. Thus the output represents the period change of the input rather than the frequency change. Since period is inversely related to frequency, this will cause distortion in the output signal. However, by operating over only a limited range a close approximation to linearity may be obtained.

In the BURSTLOCK receiver, a 200 KHz input signal is modulated up and down 15 KHz. This modulation is derived from the transmitting station's modulation of its carrier frequency, as detected by the monaural FM receiver. Over the given range the relationship between frequency f in KHz and period p in microseconds may be linearly approximated by the relationship $p = 10.035 - 0.02511f$ with an error of less than 0.5%. The relationship was found using a simple linear regression. In general, the departure from linearity increases with wider modulation and decreases as the signal frequency is increased.

5. COMPARISON OF BURSTLOCK AND THE CONVENTIONAL PLL

In addition to the well-known practical advantages of digital designs over analog designs in many applications, the BURSTLOCK circuit embodies a number of theoretical advantages over the conventional PLL. In some ways, BURSTLOCK, a second-order (single integrator) loop, may be said to combine advantages of first, second and third-order conventional loops.

Like the first-order loop, R_L and R_C are the same. However, they may be altered simply by changing the number of bits used by the local oscillator, with no effect on any other properties of the loop. Thus R_C is not reduced as the filter bandwidth is decreased. Like the third-order loop, the static phase error is zero. The response to a change in input frequency can never develop underdamped ringing, again like the first-order loop. As BURSTLOCK expects the frequency of the input to continue changing in the same direction, its action somewhat resembles the acceleration memory of the third-order loop.

The capture time of a second-order conventional loop is proportional to the square of the initial frequency difference if it is larger than the loop bandwidth. In contrast, T_C of BURSTLOCK depends only linearly on the initial frequency difference. Furthermore, decreasing the loop bandwidth increases only a constant term in the T_C value, while the same action affects T_C of the conventional loop by a cubic term. Therefore, it is less likely that sweeping will be needed to obtain rapid locking. This

improvement may be ascribed to the fact that the phase comparator does not have a periodic response.

Since BURSTLOCK contains only a small number of components, it is well suited for integration. In an integrated form it would not require the connection of external components as is usual in currently available integrated PLL's.

In the design of conventional PLL FM discriminators, it is usual to employ a post-detection filter, often a five or six-pole Bessel or Butterworth design [2]. In the BURSTLOCK receiver, only a simple RC filter might be desired to smooth out the sharp edges of the BSR output.

Due to the limitations on loop memory and the lack of a quiescent oscillator frequency, BURSTLOCK is not suitable for applications which are based on these properties, such as flywheel synchronization or the selection of one of several signals by setting f_Q close to that of the desired signal and using a small R_L . Without any f_Q , the R_L of BURSTLOCK is an absolute range rather than a deviation to either side of f_Q .

It has been seen that the signal distortion encountered in BURSTLOCK FM demodulation is inversely proportional to the filter bandwidth. This is not an unreasonable result, as it must be expected that some penalty be paid for a decrease in bandwidth. Distortion is encountered in the conventional PLL also, due to a sinusoidal phase comparator characteristic and VCO nonlinearity.

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APPENDIX

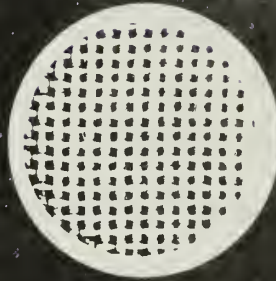
RECEIVER DESCRIPTION

Figure A.1 shows a photograph of the BURSTLOCK receiver. The front panel controls consist of a clock frequency control, clock enable and on/off switch. Mounted inside the cabinet and accessible through a port in the rear panel is an inexpensive analog radio, which provides the IF input to the BURSTLOCK circuit.

To tune in a station the clock enable switch should be set to the off position and the volume control on the radio turned up. When the desired station is tuned on the radio, the volume control should be reduced to zero and the clock enable switch set to the on position. The output from BURSTLOCK will then be audible from the speaker in the front panel. The clock frequency should be adjusted to give the best possible output.

It is necessary to use this method for tuning because it is difficult to tune the analog radio to the exact station frequency. An acceptable audio output from the analog tuner will be produced when the IF is within approximately 10% of its nominal value of 10.7 MHz. Even when monitoring the IF signal with a frequency counter, exact tuning is a time-consuming process since the frequency count deviates about the nominal value due to the modulation, and the tuning control is affected by body capacitance when adjustments are made. It is far easier to compensate for tuning errors by adjusting the clock frequency in the manner described.

BURSTLOCK



CLOCK
FREQUENCY



CLOCK
ENABLE

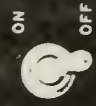


Figure A.1 Photograph of the BURSTLOCK

The components of the BURSTLOCK circuit are mounted on three printed circuit cards. The first card contains all the components shown in Fig. 4.2, with the exception of the analog tuner. The IF input is buffered with a unity-gain operational amplifier to avoid the adverse effects of loading on the tuner. Mixing is done with a 76514 doubly balanced mixer, and a 10116 comparator is used.

The second card contains all of the components shown in Fig. 4.1 except the output BSR, which is mounted on the third card. Since the BSR output produces a relatively low volume when operating directly into a speaker, a 386 audio amplifier on the same card is used to boost the signal to a more useful level. The clock generator, consisting of two 74121 monostable multivibrators and a 7406 open-collector inverter to increase the fanout, is also mounted on this card. The clock frequency is controlled by the dual 50 K Ω potentiometer on the front panel, and is variable from approximately 50 KHz to 5 MHz. The clock enable switch is connected to the enable pin of all shift registers and counters in the system.

A +5V and a -5V power supply are mounted inside the cabinet to make the receiver self-contained.

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